Abstract

A method is provided for manufacturing a buried strap contact between a transistor and a trench capacitor in a memory cell, particularly a DRAM memory cell. In this method, the two spacers of the gate electrode lying opposite one another and the gate path applied on the trench insulation of the memory cell serve as part of the mask that is employed for etching the contact trench and in which the buried bridge of the trench capacitor is subsequently generated. As a result, the position of that sidewall of the bridge facing toward the gate electrode is generated in self-aligning fashion relative to the gate electrode. This avoids photolithographic tolerances in the positioning of the bridge relative to the gate electrode.